

REMARKS

The present application was filed on July 30, 2003 with claims 1-14. Claims 1, 13 and 14 are the independent claims.

Claim 14 is rejected under 35 U.S.C. §101 as being directed to non-statutory subject matter.

Claims 1-14 are rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,278,834 (hereinafter “Mazzola”).

In this response, Applicants respectfully traverse the §101 and §102(b) rejections, and amend claim 14. Applicants respectfully request reconsideration of the present application in view of the amendments above and remarks below.

With regard to the §101 rejection, Applicants respectfully traverse on the ground that the originally-recited article of manufacture set forth in independent claim 14, comprising a machine-readable storage medium having program code stored thereon, constitutes statutory subject matter. The program code stored on the machine-readable storage medium, when executed, performs one or more steps producing a useful, concrete, and tangible result, and therefore the claim recites statutory subject matter. See, e.g., In re Beauregard, 53 F.3d 1583; 35 USPQ2d 1383 (Fed. Cir. 1995); In re Lowry, 32 F.3d 1579, 32 USPQ2d 1031 (Fed. Cir. 1994). Notwithstanding the traversal, Applicants have amended claim 14 without prejudice, solely in order to expedite prosecution of the application.

The claim as amended now refers to a processor-readable storage medium that contains processor-executable instructions. It is believed that the scope of the claim is not narrowed in any way as a result of this amendment.

With regard to the §102(b) rejection, Applicants initially note that MPEP §2131 specifies that a given claim is anticipated “only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference,” citing Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Moreover, MPEP §2131 indicates that the cited reference must show the “identical invention . . . in as complete detail as is contained in the . . . claim,” citing Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). Applicants respectfully traverse the §102(b) rejection on the ground that the Mazzola reference fails to teach or suggest each and every limitation of claims 1-14 as alleged.

Independent claim 1 is directed to a processor comprising controller circuitry and first memory circuitry internal to the processor. The controller circuitry is configurable to determine for a given protocol data unit received by the processor whether the given protocol data unit is a single-cell protocol data unit. The processor is connectable to a second memory circuitry external to the processor. Information characterizing the given protocol data unit is stored in the first memory circuitry if the given protocol data unit is a single-cell protocol data unit, and information characterizing the given protocol data unit is stored in the second memory circuitry if the given protocol data unit is not a single-cell protocol data unit.

In an illustrative embodiment of the present invention, as shown in FIG. 1, a network processor 102 comprises an internal memory 104 and is coupled to an external memory 106. The internal memory 104 includes a single-cell storage portion 122 for storing information characterizing single-cell protocol data units. The external memory 106 includes a multi-cell linked-list storage portion 124 for storing information characterizing multi-cell protocol data units. See the specification at page 5, lines 12-19.

The Examiner in formulating the §102(b) rejection argues that the limitations of claim 1 are met by the arrangement shown in FIG. 1 of Mazzola. More specifically, the Examiner argues that the recited processor is the end-system processing node 10, that the recited first memory circuitry internal to the processor is memory 14 of the end-system processing node 10, and that the recited second memory circuitry external to the processor is the stack manager 14b within memory 14. See the Office Action at page 3, first five paragraphs. However, claim 1 clearly specifies that the second memory circuitry is external to the processor. If the processor is the node 10, the stack manager 14b is not external to that processor, as would be required by the claim. Similarly, if one were to assume that the recited processor of claim 1 is the processor 12 within the node 10, memory 14 fails to meet the recited first memory circuitry. This is because claim 1 clearly specifies that the first memory circuitry is internal to the processor.

Applicants further note that the buffers referred to by the Examiner are part of buffer pool 14c within memory 14. All protocol data units, regardless of whether or not they are single-cell protocol data units, are stored in the buffers 20 that are part of the buffer pool 14c within memory 14. See Mazzola at column 5, lines 50-64. It is therefore apparent that all the protocol data units in

Mazzola are stored in the very same memory circuitry, namely the buffers 20 that are part of the buffer pool 14c in memory 14, with this memory circuitry being external to the processor 12 and internal to the node 10.

Accordingly, Applicants respectfully submit that the FIG. 1 arrangement in Mazzola, relied upon by the Examiner in formulating the rejection, fails to teach or suggest the claimed arrangements in which information characterizing a given protocol data unit received by a processor is stored in first memory circuitry internal to the processor if the received protocol data unit is a single-cell protocol data unit, and is stored in second memory circuitry external to the processor if the received protocol data unit is not a single-cell protocol data unit. Moreover, by using a memory 14 that is external to processor 12 to store all protocol data units, regardless of whether or not such protocol data units are single-cell units or multi-cell units, Mazzola appears to suffer from the very problems identified by Applicants at page 2, lines 1-13 of the specification.

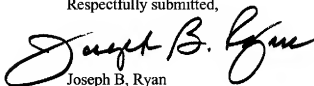
Finally, Applicant again notes that claim 1 is rejected on anticipation grounds. In order to support such a rejection, as mentioned previously herein, the cited reference must show the “identical invention . . . in as complete detail as is contained in the . . . claim.” In the present rejection, the Examiner is attributing features to the Mazzola protocol stack management method that are clearly not described in the reference and are in fact contrary to explicit teachings that are provided in the reference. Accordingly, the anticipation rejection is believed to be fundamentally flawed, and should be withdrawn.

Dependent claims 2-12 are believed allowable for at least the reasons identified above with regard to claim 1. One or more of these claims are also believed to define separately-patentable subject matter over the cited art.

Independent claims 13 and 14 include limitations similar to those of claim 1, and are believed allowable for reasons similar to those described above with reference to claim 1.

In view of the above, Applicants believe that claims 1-14 are in condition for allowance, and respectfully request withdrawal of the §101 and §102(b) rejections.

Respectfully submitted,

A handwritten signature in black ink, appearing to read "Joseph B. Ryan". The signature is fluid and cursive, with a large initial "J" and a stylized "R".

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